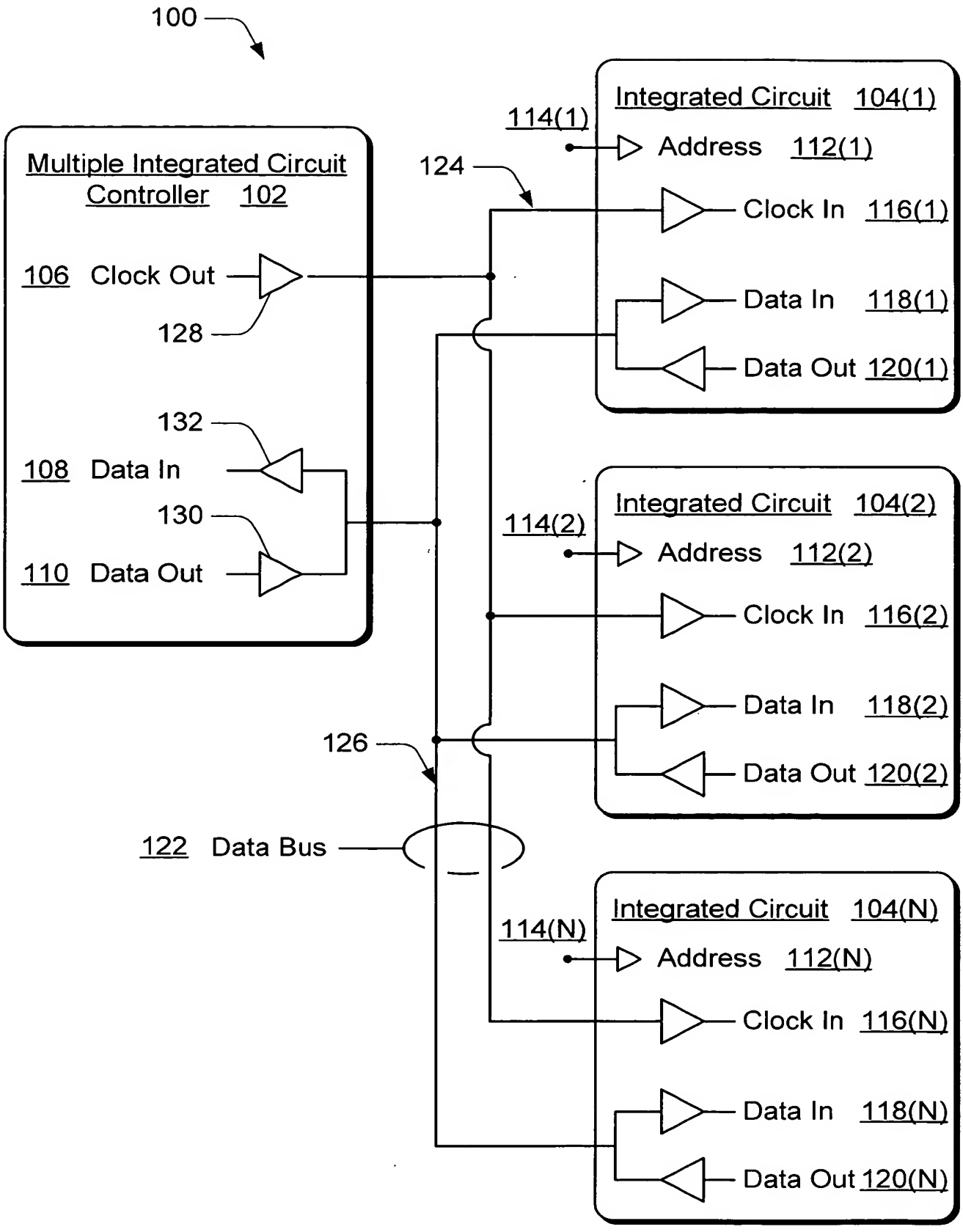
100
Multiple Integrated Circuit Controller 102
106 Clock Out
128
132
108 Data In
130
110 Data Out
124
126
122 Data Bus
Integrated Circuit 104(1)
114(1)
Address 112(1)
Clock In 116(1)
Data In 118(1)
Data Out 120(1)
Integrated Circuit 104(2)
114(2)
Address 112(2)
Clock In 116(2)
Data In 118(2)
Data Out 120(2)
Integrated Circuit 104(N)
114(N)
Address 112(N)
Clock In 116(N)
Data In 118(N)
Data Out 120(N)

Fig. 1

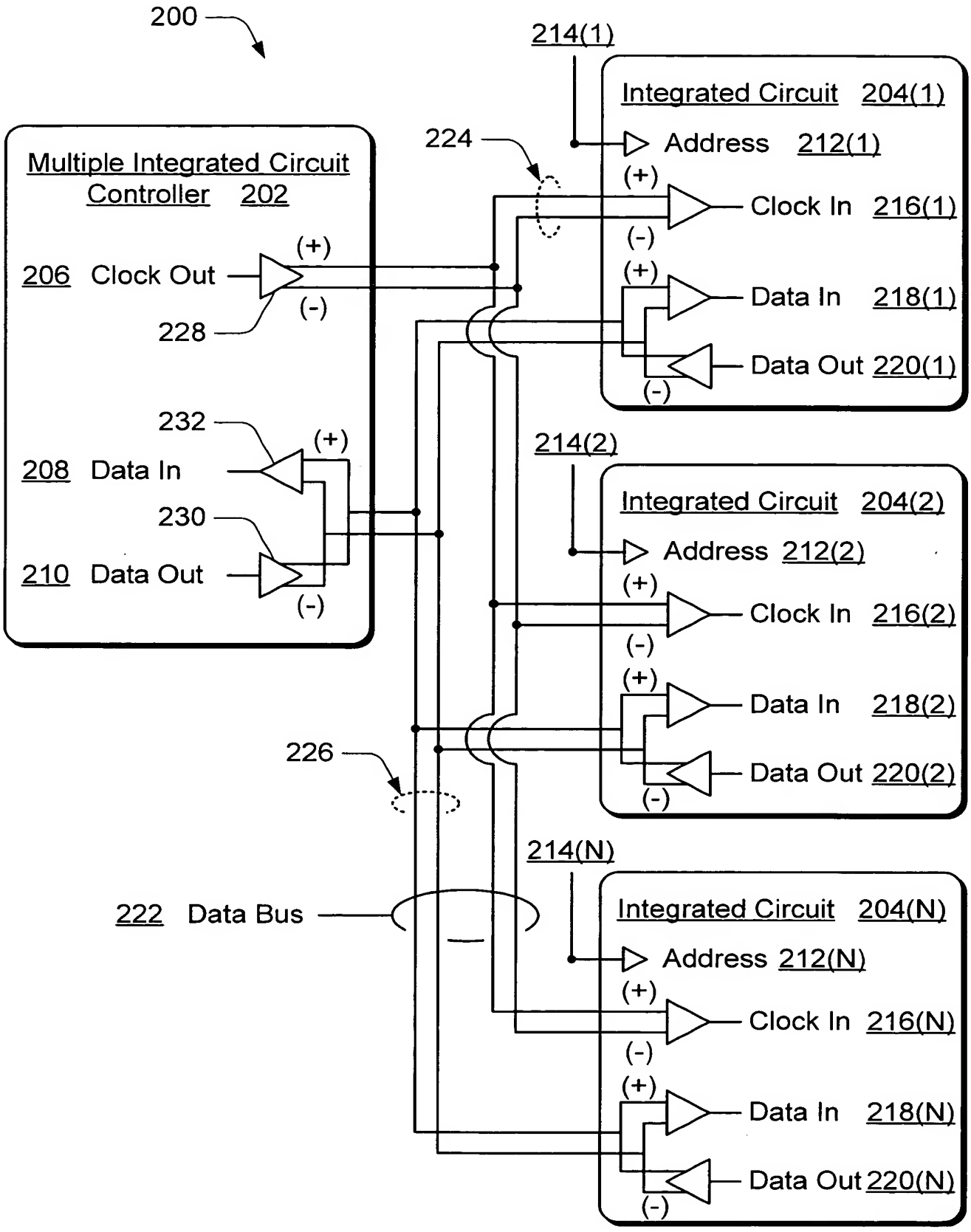
200
214(1)
Integrated Circuit 204(1)
Address 212(1)
224
(+)
Clock In 216(1)
(-)
Multiple Integrated Circuit Controller 202
(+)
206 Clock Out
(-)
228
(+)
Data In 218(1)
Data Out 220(1)
(-)
232
(+)
208 Data In
214(2)
Integrated Circuit 204(2)
230
Address 212(2)
210 Data Out
(-)
(+)
Clock In 216(2)
(-)
(+)
Data In 218(2)
226
Data Out 220(2)
(-)
214(N)
222 Data Bus
Integrated Circuit 204(N)
Address 212(N)
(+)
Clock In 216(N)
(-)
(+)
Data In 218(N)
Data Out 220(N)
(-)

Fig. 2

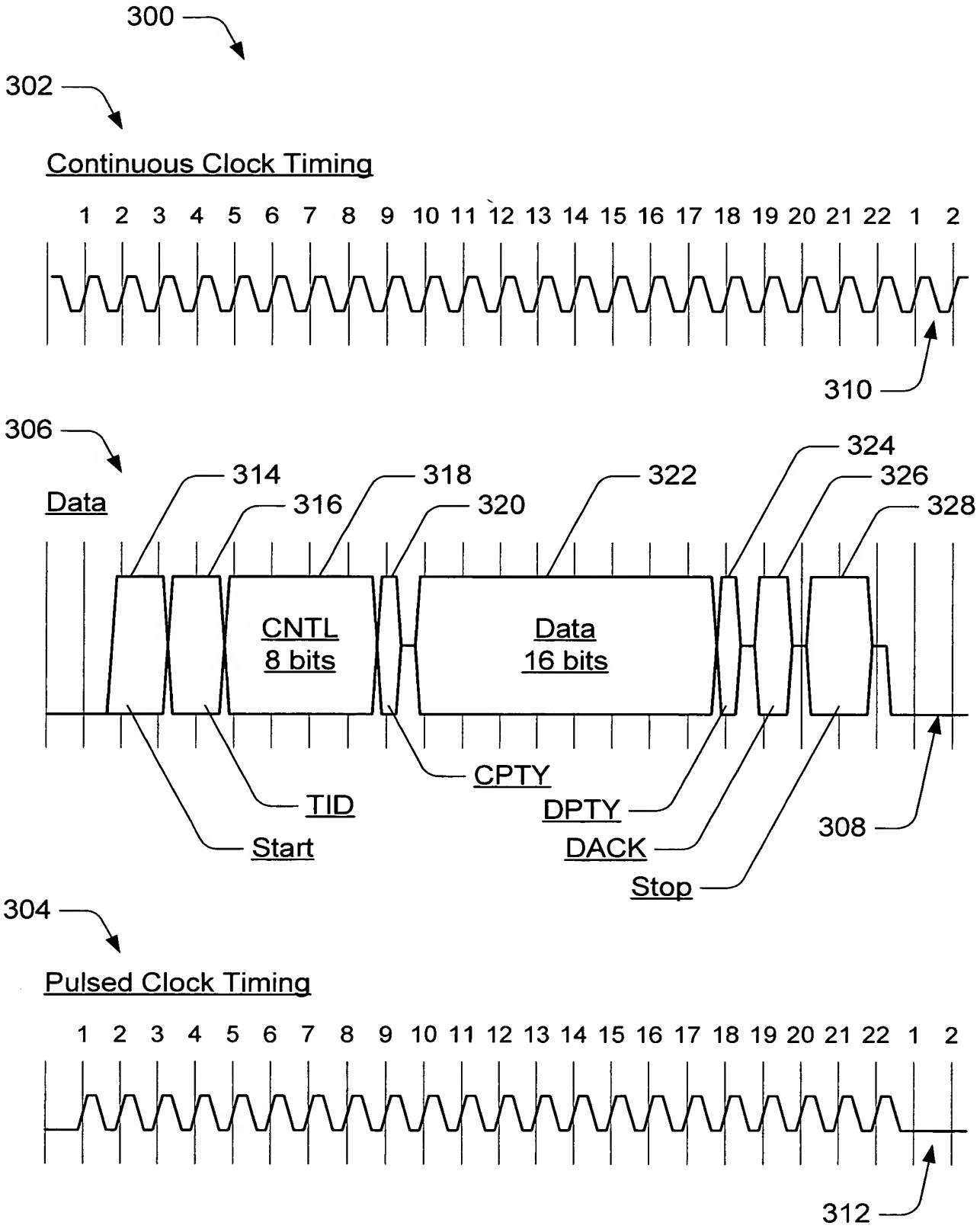
300
302
Continuous Clock Timing
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 1 2
310
306
Data
314
316
318
320
322
324
326
328
CNTL
8 bits
Data
16 bits
CPTY
TID
DPTY
DACK
Start
Stop
308
304
Pulsed Clock Timing
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 1 2
312

Fig. 3

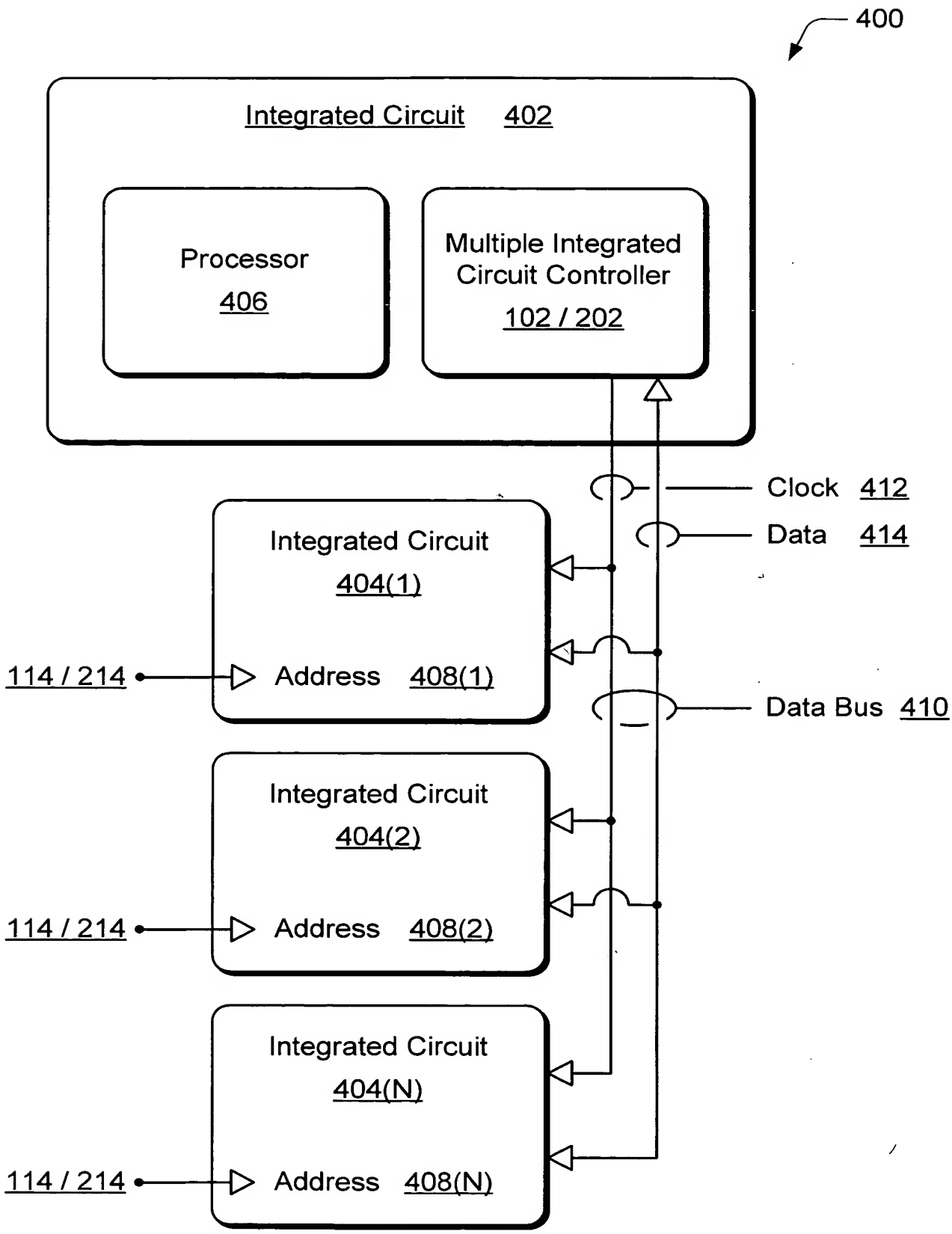
400
Integrated Circuit 402
Processor 406
Multiple Integrated Circuit Controller 102 / 202
Clock 412
Data 414
Integrated Circuit 404(1)
114 / 214
Address 408(1)
Data Bus 410
Integrated Circuit 404(2)
114 / 214
Address 408(2)
Integrated Circuit 404(N)
114 / 214
Address 408(N)

Fig. 4

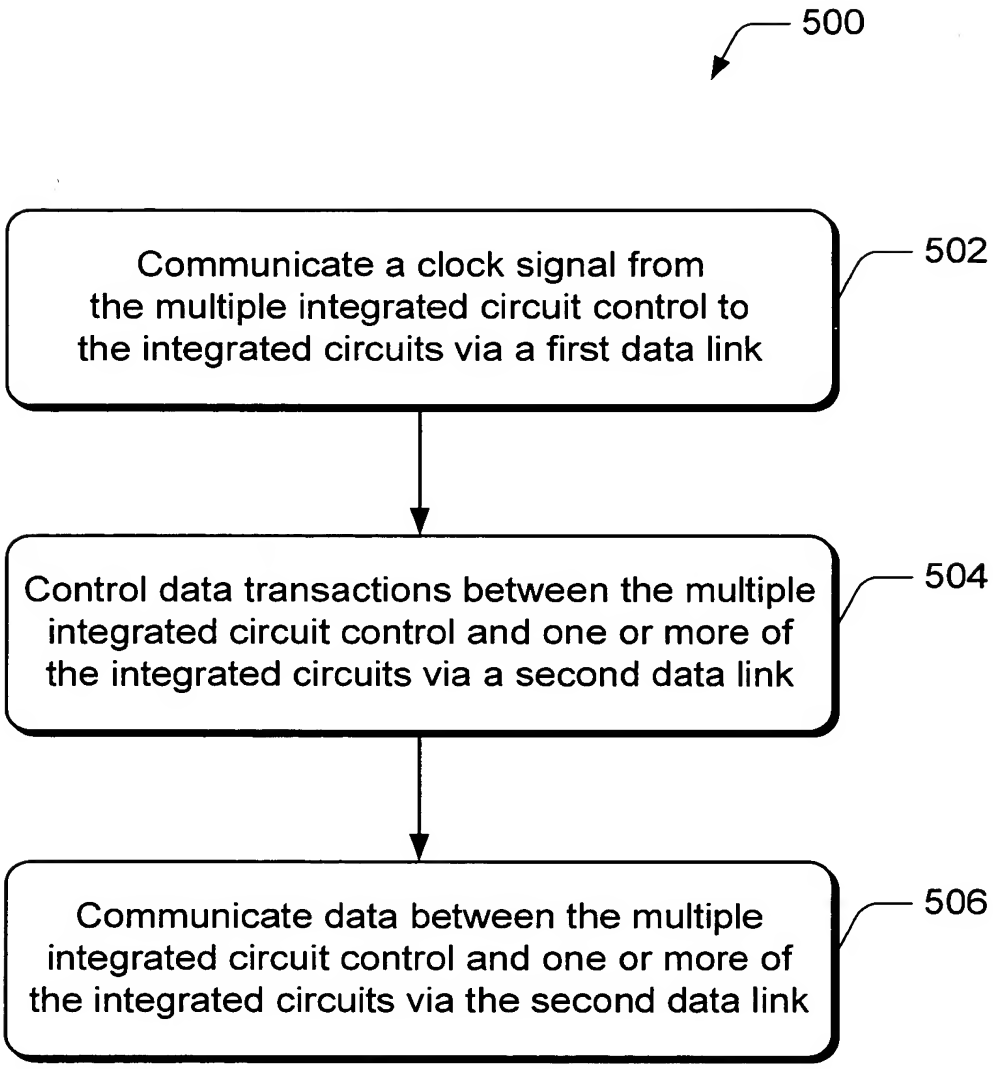
500
Communicate a clock signal from the multiple integrated circuit control to the integrated circuits via a first data link
502
Control data transactions between the multiple integrated circuit control and one or more of the integrated circuits via a second data link
504
Communicate data between the multiple integrated circuit control and one or more of the integrated circuits via the second data link
506

Fig. 5

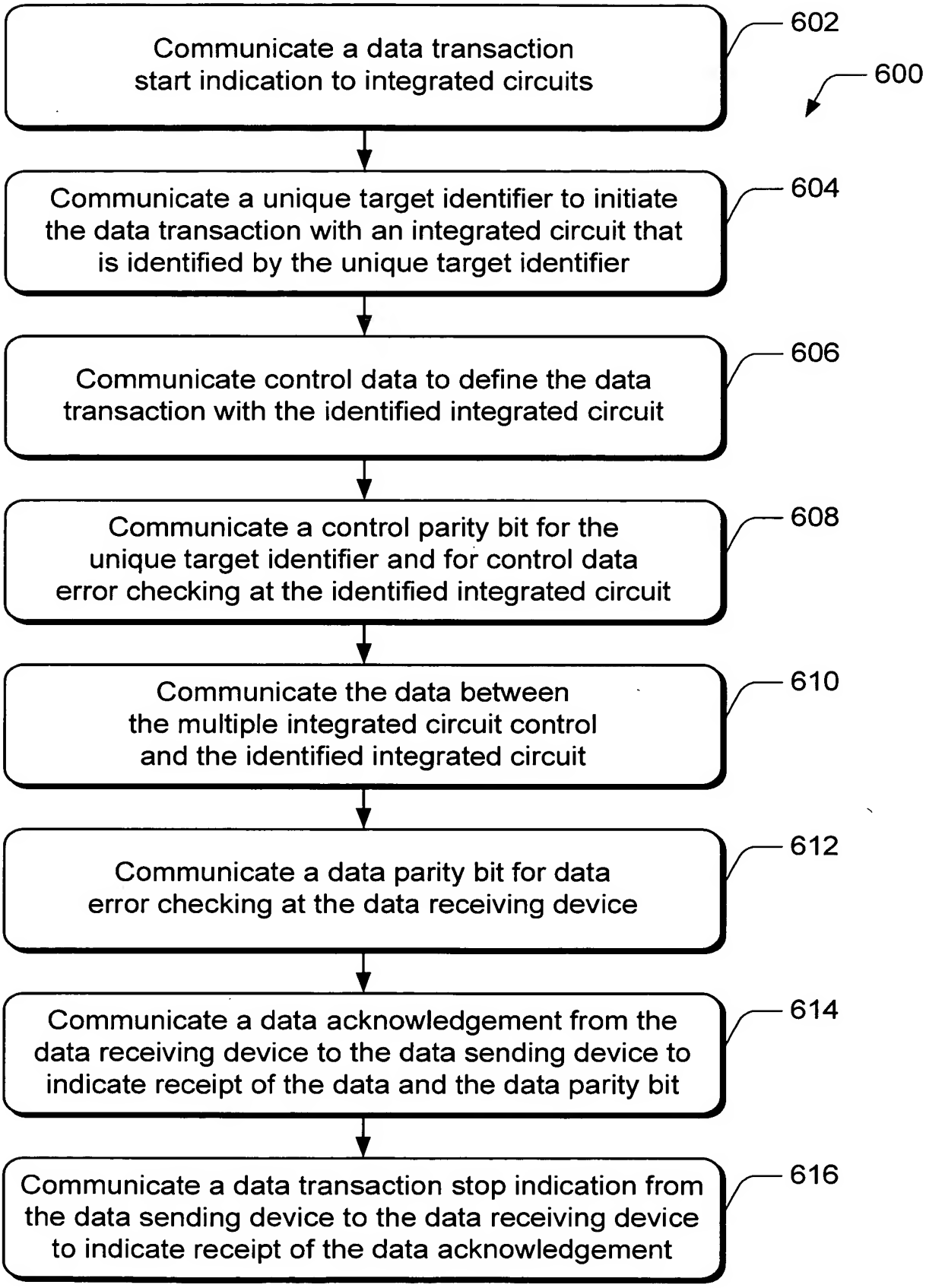
Communicate a data transaction start indication to integrated circuits
602
600
Communicate a unique target identifier to initiate the data transaction with an integrated circuit that is identified by the unique target identifier
604
Communicate control data to define the data transaction with the identified integrated circuit
606
Communicate a control parity bit for the unique target identifier and for control data error checking at the identified integrated circuit
608
Communicate the data between the multiple integrated circuit control and the identified integrated circuit
610
Communicate a data parity bit for data error checking at the data receiving device
612
Communicate a data acknowledgement from the data receiving device to the data sending device to indicate receipt of the data and the data parity bit
614
Communicate a data transaction stop indication from the data sending device to the data receiving device to indicate receipt of the data acknowledgement
616

Fig. 6

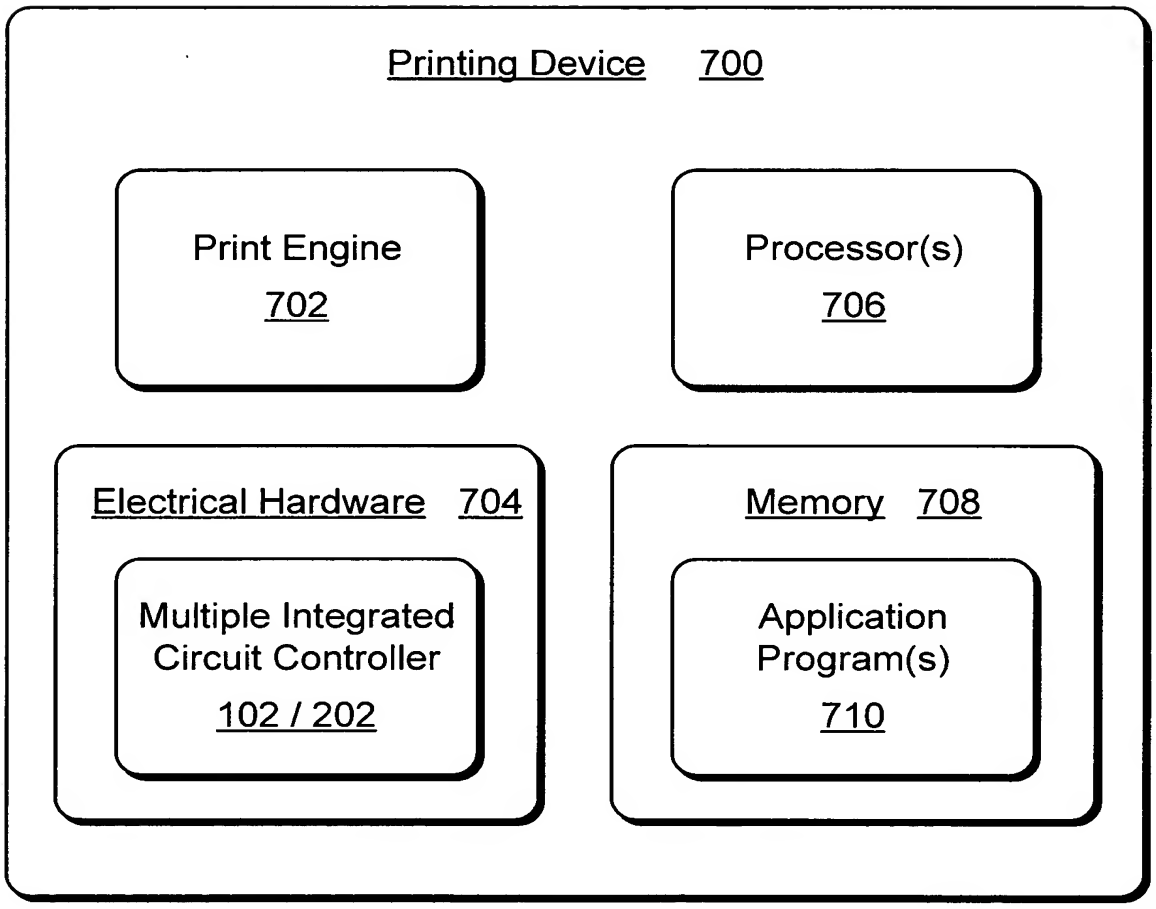
Printing Device 700
Print Engine
702
Processor(s)
706
Electrical Hardware 704
Multiple Integrated Circuit Controller
102 / 202
Memory 708
Application Program(s)
710

Fig. 7